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Hysteretic Delta-Sigma Modulator

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Abstract

This paper presents a simulation and calculation for the hysteretic delta-sigma modulator (HDSM). A complete theoretical study of the significant modulator parameters is also given. The HDSM structural design has three characteristics appropriate for the high-speed A/D conversion: (1) all signals contained by the modulator are positive for a specified enclosed input; (2) no sample-and-hold switch necessary for the reason that of using a bi-stable switch with hysteresis; (3) the input signal has almost a linear relationship with the time-averaged output.

Keywords
Delta sigma modulator, Fiber optics, Modulation, high-speed A/D,

1. Introduction

At the present time, analog to digital converting technique become an important topic in electronic system. As known, the Delta-Sigma-Modulator (DSM) is a complicated system, because it engages analog and digital problem for its implementation. Most significant fact is the practical part, since of its robustness and the number of significant applications used in the design of Analog-to-Digital Converters. The hysteretic delta-sigma modulator (HDSM) is a continuous-time delta-sigma modulator CT-DSM with binary (0, 1) output. All signals contained by the modulator are positive which composes its optical implementation practical. Structural design of the hysteretic delta sigma modulator HDSM and the input/output relation of the inverted bi-stable device are shown in Figure 1. When the parameters are chosen properly the ranges of all signals within the modulator have positive values.

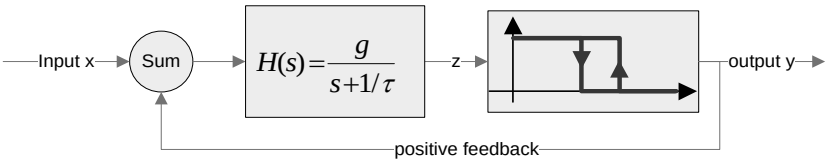

Figure 1. Hysteretic delta-Sigma Modulator (HDSM)

Figure 1 is an example of a system expressed by the following transfer function. The input/output relation of the inverted bi-stable device is shown in Figure 2 where g is a constant gain and τ is a constant delay parameter. The device hysteresis is necessary for controlling

1. The pulse spacing
2. The operational limits of the input rage.

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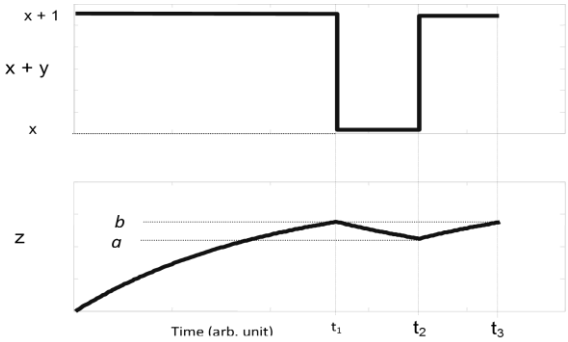

Figure 2. The input and output of leaky integrator versus time

This paper discusses a theoretical analysis of HDSM and a simulation to verify the calculation values to the simulated values. The HDSM operates with no clock signal in asynchronous mode. This paper develops equations regarding how the modulator parameters (time constant, gain, switch-on, and switch-off thresholds) relate to the sampling rate of the modulator. Since a sample-and-hold device is not used, the modulator is a true continuous-time delta-sigma modulator. However, we could define an equivalent to the sampling rate by considering a constant input to the modulator that requires the shortest time in which the bi-stable device is either on or off. In other words, the sampling rate is the inverse of the shortest output pulse width.

In keeping the theoretical development simple, we use constant input to the modulator since the sampling rate is usually much higher than the signal cut-off frequency. The
leaky integrator in a very generic form could be any system which accumulates positive inputs and leaks out at the same time. Therefore, in the case of zero input the integrator output gradually approaches zero. A simple example is a system described by the following transfer function.

$$H(s) = \frac{g}{s + 1/\tau} \tag{1}$$

Where g is a constant gain parameter and τ is a constant delay parameter. The HDSM with the simple integrator and the inverted bi-stable device is shown in Fig. 3. As we show later, the device hysteresis is essential in controlling the pulse spacing and the operational limits of the input rage. Let us assume a constant input x enters the modulator. Without loss of generality, we normalize the input by the on-state value of the bi-stable device, therefore the on-state value is assumed to be one. We will then find the corresponding output of the modulator by using the method of Laplace transform. The integrator initially is at its zero state. Therefore, the output of the bi-stable device is one, and the input to the integrator is $x+1$. The response of the integrator to this input is

$$z(t) = \tau g(x+1)(1 - e^{-t/\tau}) \tag{2}$$

This response does not change the bi-stable device output as long as $z(t) < b$. When the integrator output becomes b, at time, say t_1, the bi-stable device output y switches back to zero (see Fig. 4). Now the input to the integrator is reduced to the value x, and its response is

$$z(t) = \tau g(x+1)(1 - e^{-t/\tau}) - \tau g(1 - e^{-(t-t_1)/\tau}) \tag{3}$$

For $t_1 < t <$ next swtiching time

Note that this switching happens at $t = t_1$.The bi-stable device output stays at zero until its input reduces to a. At time, $t = t_2$, the output $y(t_2)$ switches back to one. The corresponding integrator output will be the following relation until $t = t_3$, when the $z(t)$ reaches value b.

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$$z(t) = \tau g(x+1)(1-e^{-t/\tau}) - \tau g(1-e^{-(t-t_1)/\tau}) + \tau g(1-e^{-(t-t_2)/\tau}) \quad (4)$$

For $t_1 < t_2 < t <$ next swtiching time

As long as the input stays constant, the above switching sequence of (3, 4) will repeat itself. Using (2), (3), and (4), the two important time intervals $\Delta t_{off} = t_2 - t_1$ and $\Delta t_{on} = t_3 - t_2$ are calculated as

$$\Delta t_{off} = t_2 - t_1 = \tau \ln \frac{b - \tau g x}{a - \tau g x} \quad (5)$$

$$\Delta t_{ON} = t_3 - t_2 = \tau \ln \frac{\tau g x + \tau g - a}{\tau g x + \tau g - b} \quad (6)$$

Where

$$a = \tau g(x+1)(1 - e^{-t_2/\tau}) - \tau g\,(1 - e^{\frac{-(t_2 - t_1)}{\tau}}) \quad (7)$$

$$b = \tau g(x+1)(1 - e^{-t_3/\tau}) - \tau g\,(1 - \frac{e^{-t_3/\tau}}{e^{-t_1/\tau}}) + \tau g\,\left(1 - \frac{e^{-t_3/\tau}}{e^{-t_2/\tau}}\right)$$

The input and output of the integrator versus time are shown in Figure 2. We can visualize our results so far in figure 3, where the output is periodic with a period of $\Delta t_{OFF} + \Delta t_{ON}$. In demodulating the signal, a low-pass filter is used. In our case of the constant input, the low-pass filter can be an average-pass filter (a low-pass filter with cutoff frequency at zero or a digital counter). Therefore, all we need to detect is the average of the signal given by

$$\langle y(t) \rangle = \frac{\Delta t_{on}}{\Delta t_{on} + \Delta t_{off}} \quad (8)$$

We can visualize our results so far in Figure 3, where the output is periodic with a period of $\Delta t_{OFF} + \Delta t_{ON}$. In demodulating the signal, a low-pass filter is used. In our case of the constant input, the low-pass filter can be an average-pass filter (a low-pass filter with cutoff frequency at zero or a digital counter).

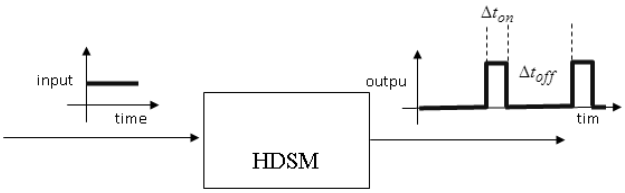

Figure 3. The Response Of The HDSM To A Constant Input

3. Simulation

All simulations in this paper are done using MATLAB/Simulink. We use a sinusoidal signal input of the following form

$$x(t) = 0.3\sin(2\pi t) + 0.5 \quad (9)$$

We design this system to verify the results obtained from the equations developed in the previous section. In the system, we add delay in the form of positive feedback delay. The relay operating limits is set to on point of 0.45 and off point of 0.55. We need to highlight that the operation of the relay in the MATLAB/Simulink requires the switch on point value to be greater than or equal to the Switch off point. In our Reverse HDSM model, we require the switch on point to be smaller than the switch off point. To satisfy this condition we employ two relays and set each of them as an off point and the on point. In order to follow a simplistic scheme, we set up the condition in the loop that the system should turn on when it reaches 0.45 and when it reaches 0.55 it should turn off. The loop is executed based on the output received from the derivative, for all positive values, the relay turns on but for the negative values the relay turns off. The value of the derivative is set at default value to obtain zero linearization. For each simulation step we take the derivative of the input signal. Figure 4 shows the output of binary delta sigma modulator BDSM [1]

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corresponding to a sinusoidal input while Figure 5 shows the output of R-HDSM. We also see the change in behavior of the system, when sinusoidal input and the delay vary. The corresponding $\Delta t_{on}$and Δt_{off} periods of the system change accordingly when the delay of the system is increased. We also perceive that with the increasing of the delay in the system, the $\Delta t_{on}$and Δt_{off} periods are seen to be much longer. Result from simulation was almost same as the result collected from the theoretical part. The simulation shows that R-HDSM is faster than BDSM with 36%. This result will help at Ultra high speed A/D conversion for optical high-speed implementation.

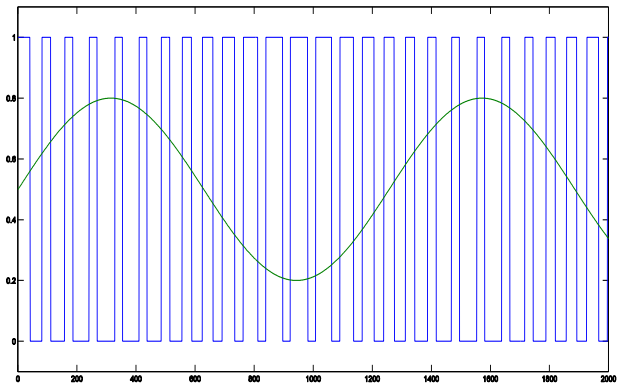

Figure4. output of BDSM corresponding to a sinusoidal input

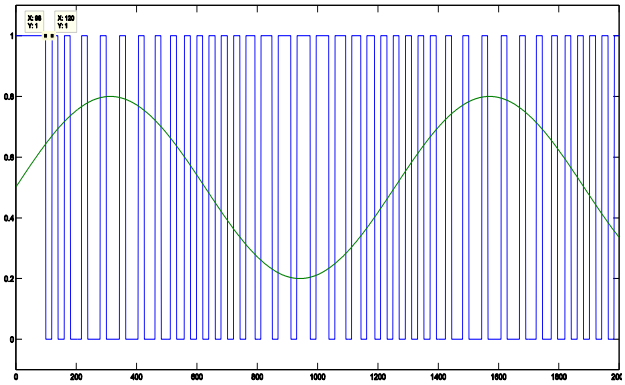

Figure5. output of R-HDSM corresponding to a sinusoidal input

4. Summary

The theoretical analysis for reverse hysteretic delta sigma modulator to characterize the input signal bounds and switching time using the parameters of the modulator were presented. We implemented R-HDSM using MATLAB/Simulink and derived a relationship between the theoretical switching time and the obtained results from simulation. The simulation results confirm the theoretical expectations. The results presented that the amount of time required for switching in case of a reverse HDSM is much less compared to the ordinary HDSM. This can be explained based on the fact that, the operation of the HDSM involves switching of the bi-stable device at a point further away than the R-HDSM. For HDSM, the system switches on at b whereas in case of Reverse HDSM, the system switches on at a, hence the amount of switching time is reduced by more than 36%. This result can be aimed at ultra-high speed A/D conversion for optical high-speed implementation. Moreover, the signals in the modulator are nonnegative making the optical implementation possible.

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Biography

Raed Althomali currently is the Head of Electrical and Electronics Engineering Technology Department at Yanbu Industrial College, Saudi Arabia. He earned a Ph.D. in Electrical and Computer engineering in fiber optics and photonics, USA in 2014. His main areas of research interest are signal processing, all-optical devices, active filters, neural networks, renewable energy and Electrical machine. Dr. Raed is a member of the Saudi Council of Engineers and Optical Society of America.

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