

Corner Effects in SOI Vs Bulk Tri gate FinFETs using 3D device simulation

Santosh K. Gupta and Pavan K. Manchi

**Department of Electronics and Communication Engineering
National Institute of Technology, Silchar (Assam) – 788010, India**

Abstract

SOI FinFET transistors have emerged as novel devices having superior controls over short channel effects (SCE) than the conventional MOS transistor devices. However despite these advantages, these also exhibit certain other undesirable characteristics such as corner effects, quantum effects, tunneling etc. Usually, the corner effect deteriorates the performance by increasing the leakage current. In this work, the corner effect of SOI and Bulk Tri-gate FinFETs are investigated by 3D device simulation and their electrical characteristics are compared for different body doping and bias conditions. The corner effect in small size SOI tri gated FINFETS for typical device parameters does not deteriorate the performance and an enhancement in the on state current and sub-threshold performance have been observed. In corners due to charge sharing effects between two adjacent gates, causes premature inversion in corners and produces high drain current in case of SOI tri gate FinFETs.

Keywords

SOI, SCE, corner effect, Tri gate-FINFET, premature inversion.