Improvement in Harmonic Distortion using Seven level H-Bridge VSI Topology based Dynamic Voltage Restorer

Ir. Dr K Chandrasekaran
Assistant Professor
University Tunku Abdul Rahman
Kampar. Malaysia.
E-mail: kchandra@utar.edu.my
Contact no. 019-5584754

Ir. Dr V.K. Ramachandaramurthy
Professor
University Tenaga Nasional
Bangi. Malaysia.
E-mail: vigna@uniten.edu.my

Abstract

This paper exhibits the model, the control and simulation of H-Bridge VSI topology based Dynamic Voltage Restorer (DVR). The structure and the operating principle of the Cascaded H-Bridge Seven level Inverter is realized. The phase shifted SPWM was adapted to reduce the lower order harmonics of the output voltage. The controller was based on the dqo transformation. The performance of the proposed method was affirmed in PSCAD. The simulation results are evaluated and discussed. The controller was able to manage the zero-sequence voltage during unbalance fault period. The phase shift SPWM was incorporated with low frequency and subsequently, the switching loss was low. The Total Harmonic Distortion (THD) with the designed DVR was significantly low in comparison to other traditional models and was within the IEEE Standards 519-2014. The envisioned controller algorithm provides excellent voltage improvements.

Keywords

DVR, Phase shifted Pulse width modulation (PSPWM), Voltage source inverter (VSI), Voltage harmonics, Voltage sag.

1.0 Introduction

Voltage sag is the most common power quality problem in an electrical network. Voltage sag is a short duration (10 ms to 1 minute) event where there is a reduction in r.m.s voltage magnitude across the load. The two parameters are sag magnitude and duration. The voltage sag ranges from 10 % to 90 % of nominal voltage (which corresponds to 90 % to 10 % remaining voltage) with a duration from half a cycle to 1 min. Voltage sag is caused due to a fault in the utility system, a fault at the customer's end or a starting a large motor or transformer energizing. The most common faults are single-phase faults account to 80 %, followed with two phases fault and two phases fault to ground. Large fault current results in a voltage drop across the network impedance. The voltage in the faulted phases drops close to zero. A voltage swell condition occurs when the voltage of one or more phase rises above the specified tolerance for a short period of time. Harmonics distortion is due to nonlinear loads. The main advantage of multilevel inverters is that the output voltage can be generated with low harmonics. The harmonics decrease proportionately to the inverter level. There are numerous types of multilevel inverters: cascaded H-bridge (CHB), neutral point clamped, flying capacitor. The CHB inverters are being widely used because of their modularity and simplicity. Various modulation methods can be applied to CHB inverters. CHB inverters can increase the number of output voltage levels by increasing the number of H-bridges. Hence, voltage imperfections in the network cannot be tolerated for most industrial applications due to down time and production losses. Thus, this motivated to develop a simple innovative hybrid DVR to cater for the voltage imperfections in the 400 Volts network. This paper demos a new Hybrid DVR with a dqo controller based CHB multilevel inverter for the harmonics and voltage sag and voltage harmonics mitigation. The advantages of this arrangement, the voltage levels can be increased, low switching losses, hybrid

filters and higher order harmonic elimination. This Hybrid DVR is cost effective alternative compared with other commercially available custom power devices and can be used in both the industrial as well as academic purposes.

1.1 Objectives

i. Develop an innovative Hybrid DVR model to mitigate the voltage imperfections in a 400 Volts network.
ii Investigate the unique dqo transformation controllers.

2.0 Literature Review

Many researchers have proposed (Kannan Kartik and J.E. Quaicoe 2000) (Hideaki Fujita and Hirofumi Akagi 1991) voltage sag mitigation and voltage harmonics compensation methods independently by using series active power filter and tuned shunt passive LC filters as a hybrid integrated model. The proposed control scheme in (Bhim Singh, et. al. 2015) is effective in compensating voltage sag and harmonics when a bank of tuned shunt passive LC filters connected at the load end are used along with a series active filter. In this case, the series active power filter improves the harmonic filtering characteristic of shunt passive LC filter. The LC harmonic filter will divert the load current harmonics to the ground, thus preventing the voltage waveform distortion at the point of common coupling (PCC). However, the improvement in THD level of voltage at the load end is not clearly established.
The control scheme in (Kannan Kartik and J.E. Quaicoe 2000) is based on the d-q algorithm. The main drawback here is the use of tuned shunt passive LC filters for current harmonics filtering which either trap or block the harmonic currents from returning to the source. Since the passive filters needs to be tuned to the specific harmonics, the line impedance must be known. Furthermore, a passive harmonic filter may excite system oscillations. Two delay units used to generate balanced 3-phase voltages for d-q transformation in the proposed controller might result in slow response. The controller is not tested for different types of faults such as balanced and unbalanced faults, balanced and unbalanced faults with harmonics generating loads, as well as harmonics alone. Also, the simulation results in various faults that are not presented or discussed.
This research proposes an innovative controller based on the Synchronous Rotating Reference Frame (SRRF) enabling the DVR to operate in the unbalanced and distorted supply conditions. With the improved scheme, the proposed DVR model will be able to achieve an improved voltage swell and sag mitigation as well as compensation of voltage harmonics, subsequently with a low THD level. This research project can provide better results in terms of the THD level and simplicity as compared to the conventional model explained in the literature. This would provide valuable input to the academics and solutions on power quality improvements to the industrial and the commercial sectors.

3.0 Modelling of DVR

3.1 Principle of DVR

The objective of the control system is to manage the load voltage during supply system voltage disturbances. The controller is to detect the voltage imperfections such as voltage sag, swell, and voltage harmonics and inject voltage deviation by providing appropriate switching strategies for the inverter. A constant magnitude load voltage is maintained by the proposed controller under the balanced and unbalanced dynamic power quality disturbances.

The control strategy of DVR should satisfy the following criterions:

- Reliable and fast response for both the transient states and steady states.
- Compensation for various types of sags and for different load connection.

Robustness for nonlinear load conditions, sudden load changes and system parameter variations. The DVR is shown in Figure 3.0. Features consists of an injection transformer whose primary is connected in series with the supply line, a PWM-VSI which is connected in series with the secondary side of injection transformer, dc supply, and a passive filter. The dc-link with a constant voltage across the capacitor provides the active and reactive power during the voltage sag.

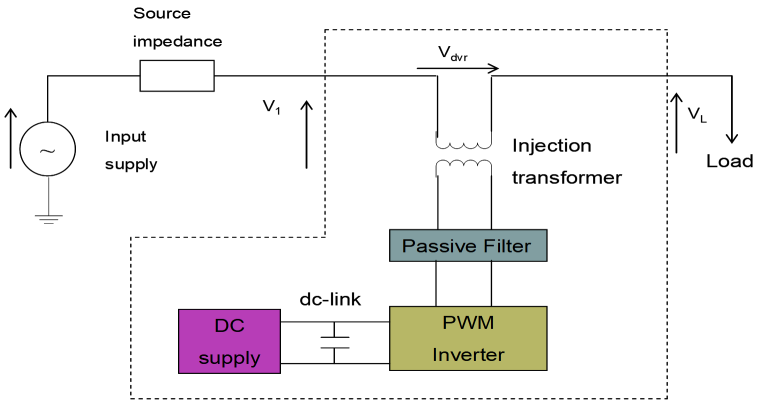


Figure 3.0. Schematic diagram of DVR

3.2 Control design

3.2.1 Synchronous rotating reference frame (SRRF) controller algorithm

In the d-q based controller algorithms, the measured system voltage will be transferred into Stationary Reference Frame using Clarke transformation, and then transferred into Synchronous Rotating Frame using Park transformation. The reference compensation voltages to control DVR are generated by comparing the calculated desired system voltages and the measured load side voltages. The error signals are subjected to a phase shift multicarrier SPWM controller to determine the desired switching pattern for the IGBTs of DVR. The developed innovative SRRF controller is simplicity to implement, required minimum components and fast response. The innovative control strategy is shown in Figure 3.1.

The input supply voltage (Vas, Vbs, Vcs) contains both the fundamental as well as the distorted components. Since, the supply voltage is distorted, a phase locked loop (PLL) is used to achieve synchronization with the supply voltage. The error signals are Vaf1, Vbf1, Vcf1.

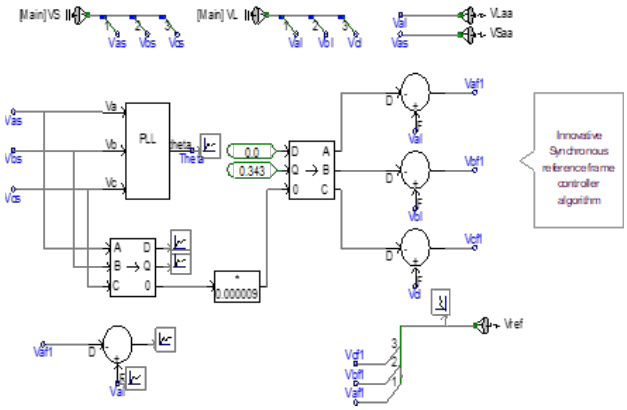


Figure 3.1. Synchronous reference frame controller algorithm.

3.2.2 Control scheme for power measurement

A simple and efficient control scheme has been designed for the various power measurements as shown in Figure 3.2. This control is based on the Clarkes transformation theory.

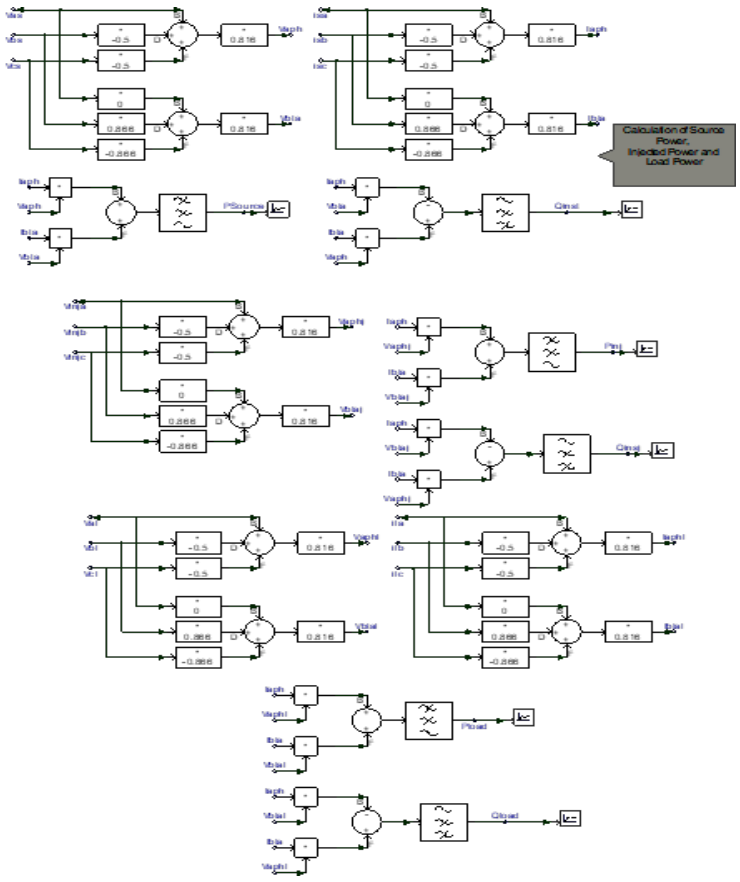


Figure 3.2. Mathematical based control scheme for power measurement

3.2.3 PSCAD implementation of cascaded H-BRIDGE multilevel inverter

The approach used in (Zhongdong Yin and Lixia Zhou 2005), (Steven M. Hietpas 2000), (Sunil Kumar Gupta 2010), (A.Venkatakrishna 2014) to implement the cascaded H-BRIDGE multilevel inverter is described. The PSCAD model of the three-phase inverter for the DVR system is shown in Figure 3.3. The converter topology is based on the series connection of single-phase inverters with separate dc sources. The structure of separate dc sources is well suited for various renewable energy sources such as fuel cell, photovoltaic. Each phase has three series connected H-bridge cell. Each cell will have four power switches with anti-parallel diodes and dc power supply. The CHB inverter in Figure 3.3 can produce phase voltages with seven voltage levels. There are six carrier signals. Three of them are applied across the positive half cycle of the modulating signal. The remaining three of them are applied across the negative half cycle of the modulating signal. From these signals twelve PWM signals are generated and then injected to the twelve switches of a leg. Same way the pulses are generated for next two phases. From Figure 3.3, when the switches S15, S15, S13, S13 and S11, S11 conducts, the output voltage of the H-bridge cells c1, c2 and c3 is Vc1 = Vc2 = Vc3 = E = Vdc, and the resultant phase voltage of the inverter is Van = Vc1 + Vc2 + Vc3 = 3Vdc. The resulting phase voltage is integrated by the addition of the voltages generated by the different cells. In similar fashion, when switches S16, S16, S14, S14 and S12, S12 is switched on, the output voltage is Van = -3E = -3Vdc. The remaining three voltage levels are +Vdc, +2Vdc, 0, and -Vdc, -2Vdc responding to the various switching states are exhibited in Table 3.0.

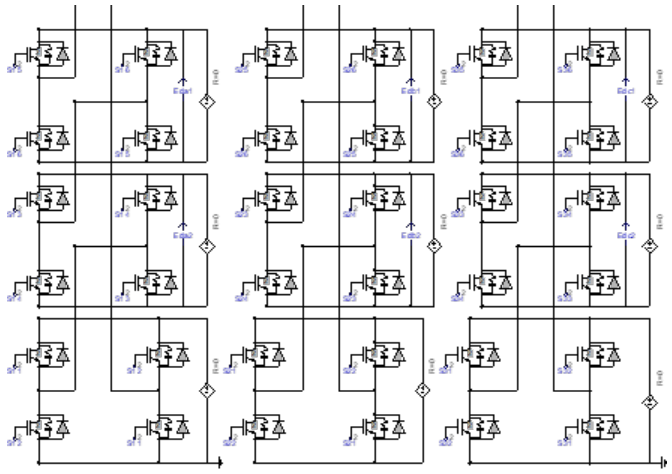


Figure 3.3. The PSCAD model of the three-phase inverter for the DVR system

Table. 3.0

Switching states of 7 level inverter

Volt	Switching states											
	S15	S15	S16	S16	S13	S13	S14	S14	S11	S11	S12	S12
+Vdc	1	1	0	0	0	1	0	1	0	1	0	1
+2Vdc	1	1	0	0	1	1	0	0	0	1	0	1
+3Vdc	1	1	0	0	1	1	0	0	1	1	0	0
0	0	1	0	1	0	1	0	1	0	1	0	1
-Vdc	0	0	1	1	0	1	0	1	0	1	0	1
-2Vdc	0	0	1	1	0	0	1	1	0	1	0	1
-3Vdc	0	0	1	1	0	0	1	1	0	0	1	1

The Phase Shifted Carrier SPWM is displayed in Figure 3.4. The unfiltered set of pulses generated by the inverter for phase A is as shown in Figure 3.5. The single-phase output voltage is displayed in Figure 3.6. The interface of the control signal and the triangular signal will boost the number of pulses per cycle and ultimately minimize the lower order harmonics (N.H. Woodley 2000).

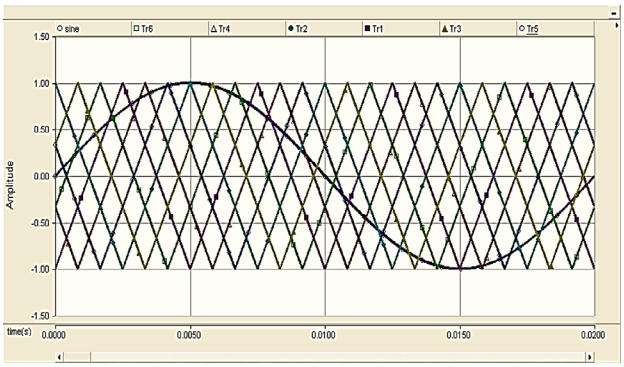


Figure 3.4. The Phase Shifted Carrier SPWM

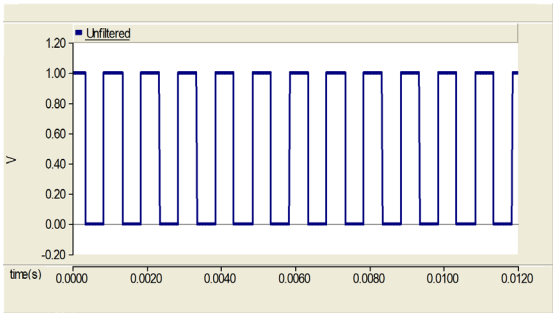


Figure 3.5. Phase A PWM Output Pulses

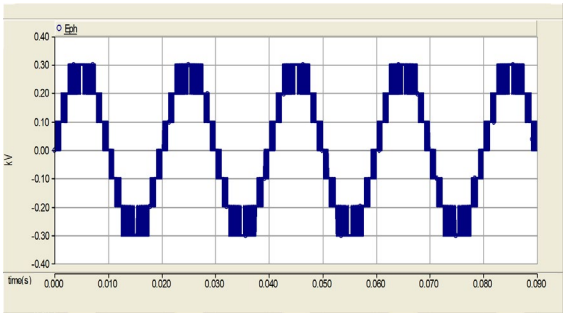


Figure 3.6. The single-phase output voltage of 7-level multilevel inverter

3.2.4 Proposed seven level control circuits.

The phase shift between any two adjacent carrier waves as expressed by Equation 2.0.

$$\varphi shift = 3600 / (m-1) \qquad \text{(Equation 3.0)}$$

The PWM signals for controlling the IGBTs of m-level multilevel converter will be generated when comparing the modulating wave with the carrier waves. The pulse generation circuit is shown in Figure 3.7. For the triangular wave, the frequency is set at 4650 Hz, and the duty cycle is 50 %, maximum and minimum output level is +1 and -1, respectively for optimum operation and to minimize the harmonics. The pulse generation is crucial to initiate the VSI gate switches. The appropriate pulse pattern is needed to generate the appropriate 7-level output staircase waveform.

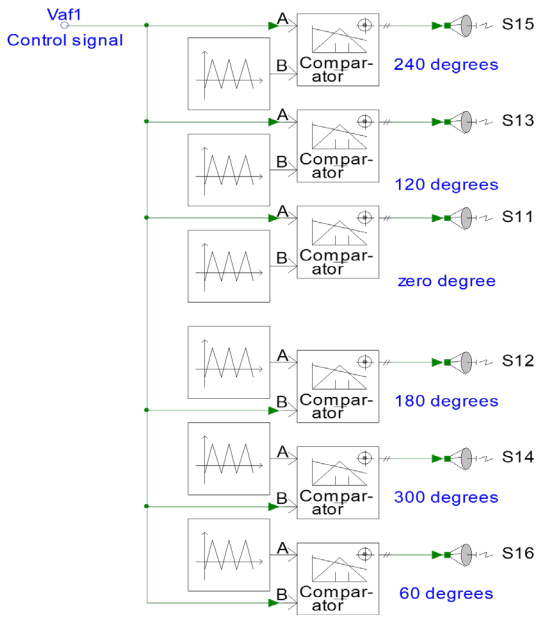


Figure 3.7. Single pole pulse generation circuit in PSCAD

The reference signal wave is compared with the six triangular carriers of same frequency and magnitude generated from the phase shift technique. When the reference signal surpasses the carrier, instant pulses are synthesized to prompt the switch to the 0N state. As illustrated in Figure 3.7, six triangular carrier waves are required with a 60 degrees phase displacement between any two adjacent carriers (Sasitharan S 2008), (Mahinda Vilathgamuwa and S.S.Cho 2002), (H. Tiwari and S. Kumar Gupta 2010).

3.2.5 Simulation of Seven Level Cascade Inverter

The 7-level inverter has six carrier signals. From these signals twelve PWM signals are generated and sent to the twelve switches of a leg. Equally the pulses are triggered for the next two phases. The modulating signal is phase shifted by 60 degrees. The maximum output line voltage of 7-level cascaded inverter is 600 Volts, as shown in Figure 3.8.

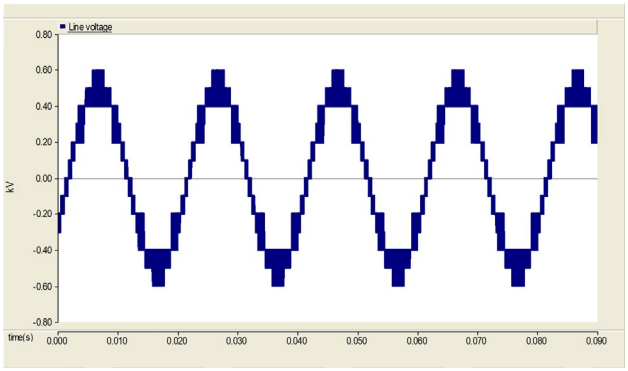
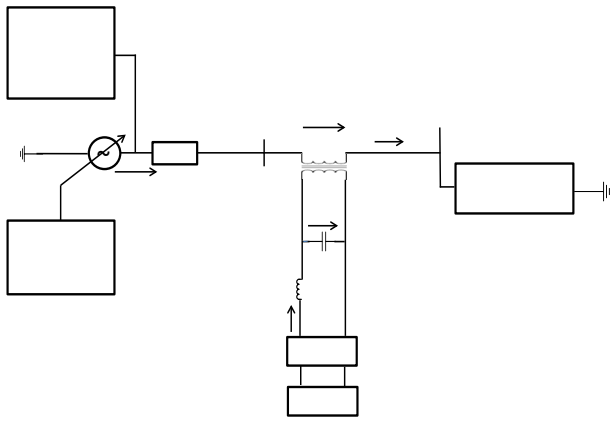


Figure 3.8. Line voltage of 7-level cascaded inverter

3.2.6 Harmonics compensation

In the steady-state conditions, the harmonic currents generated by the main nonlinear load will cause a voltage drop across system impedance and distort the supply voltage, V_S and the voltage at the sensitive load, VLoad as shown in Figure 3.9.



3.9. Single line diagram to represent power quality problem.

The voltage at the load VLoad consists of the fundamental and the harmonic voltage components.
In Figure 3.9, distorted voltage V_S will appear on the upstream source-side of the sensitive load and the phase voltages can be expressed as

$$V_{\text{sa}} = \sum_{n=1}^{\infty} \begin{bmatrix} V_{\text{on}} + V_{1n}\sin(n\omega_0 t + \varphi_{1n}) \\ + V_{2n}\sin(n\omega_0 t + \varphi_{2n}) \end{bmatrix} \quad \text{(Equation 3.1)}$$

$$V_{\text{sb}} = \sum_{n=1}^{\infty} \begin{bmatrix} V_{\text{on}} + V_{1n}\sin\left(n\omega_0 t + \varphi_{1n} - 2n\frac{\pi}{3}\right) \\ + V_{2n}\sin(n\omega_0 t + \varphi_{2n} + 2n\frac{\pi}{3}) \end{bmatrix} \quad \text{(Equation 3.2)}$$

$$V_{\text{sc}} = \sum_{n=1}^{\infty} \begin{bmatrix} V_{\text{on}} + V_{1n}\sin\left(n\omega_0 t + \varphi_{1n} + 2n\frac{\pi}{3}\right) \\ + V_{2n}\sin(n\omega_0 t + \varphi_{2n} - 2n\frac{\pi}{3}) \end{bmatrix} \quad \text{(Equation 3.3)}$$

V_{on} is zero phase sequence voltage component.
V_{1n} and φ_{1n} are magnitude and phase of positive sequence voltage component.
V_{2n} and φ_{2n} are magnitude and phase of negative sequence voltage component.
The distorted voltage at the sensitive load end is undesirable. The desirable voltage V_L at the sensitive load comprises the fundamental components as Equation (3.1) - (3.3).

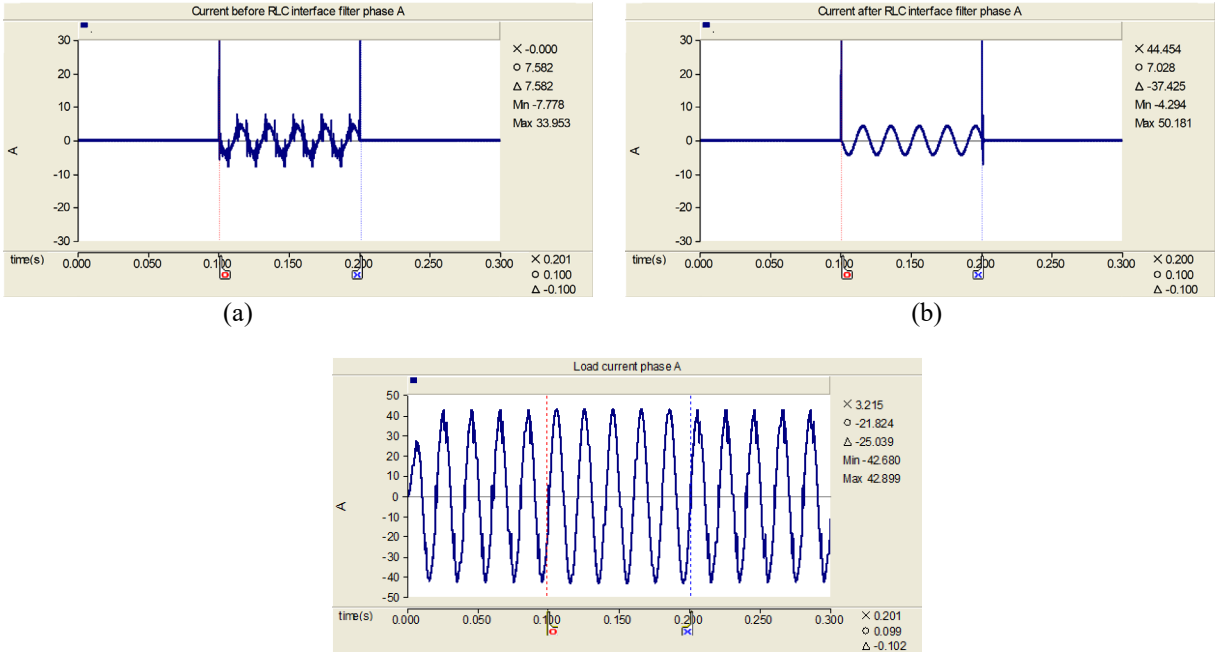
$$V_{\text{La}}^{`} = V_{11}\sin(\omega_0 t + \varphi_{11}) \quad \text{(Equation 3.4)}$$
$$V_{\text{Lb}}^{`} = V_{11}\sin(\omega_0 t - 2\frac{\pi}{3} + \varphi_{11}) \quad \text{(Equation 3.5)}$$
$$V_{\text{Lc}}^{`} = V_{11}\sin(\omega_0 t + 2\frac{\pi}{3} + \varphi_{11}) \quad \text{(Equation 3.6)}$$

The voltage that is injected by the DVR will compensate for the difference between V_S and the desired voltage VLoad described by Equation (3.4) - (3.6). The injected voltage by the DVR will contain both the ac voltage component in series with the distorted supply voltage V_S and contains the entire harmonic component as Equation (3.1) - (3.3). Equation (3.1) - (3.3) express in compact expression:

$\vec{V}_{\text{s}} = [V_{\text{sa}}, V_{\text{sb}}, V_{\text{sc}}]^{\text{T}}$ and Equation (3.4) - (3.6) denoted by $\vec{V}_{Lf} = \left[V_{\text{La}}^{`}, V_{\text{Lb}}^{`}, V_{\text{Lc}}^{`}\right]$

Let V_{Lh} be the vector containing all the harmonic components in Equation (3.1) - (3.3).
Hence from Equation (3.1) - (3.3), the injection voltage V_{inj} from the DVR to compensate would have to be
$V_{inj} = - V_{Lh} = V_{Lf} - VLoad$ (Equation 3.7)

V_{Lf} is the fundamental voltage component. The injection voltage V_{inj} that is generated will be used to mitigate the harmonic distortions. From Figure 3.9, L_f filters the high-frequency harmonic voltage components. Low order harmonics (5^{th}, 7^{th}, 11^{th} and 13^{th}) are due to the nonlinearity between the IGBTs in the same leg, the voltage drop during the on-state of IGBTs and also distortion in the supply voltage (Suresh Kumar 2015).
Figure 3.10(a) represents the injected current phase A before the RLC interface filter. This current is distorted. Figure 3.10(b) represents the injected current phase A after the RLC interface filter. Between the intervals 0.1 to 0.2 sec, the current is minimum distortion less. Figure 3.10(c) represents the load current phase A with the DVR in operation.



(a) (b)

(c)

Figure 3.10. Injected current Phase A
(a) before RLC interface filter
(b) after RLC interface filter
(c) load current Phase A

3.2.7 Swell compensation

The control algorithm for voltage swell is shown in Figure 3.11. The voltage swell is created at the main source supply

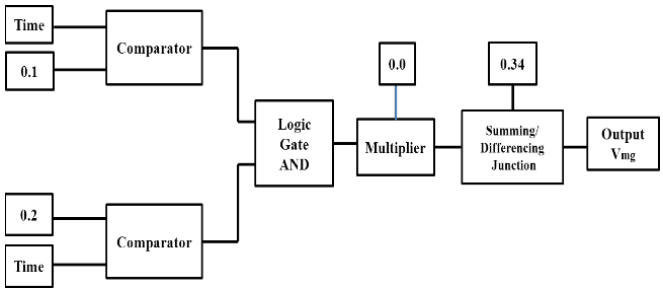


Figure 3.11. Algorithm for voltage swell

4.0 Results and Discussion

PSCAD/EMTDC was adapted to verify the effectiveness of the proposed control technique. The distribution system is rated at 400 Volts delivering a sensitive load of 29.5 kVA. The filter resistor, inductor and capacitor values have been determined for this application on the assumption that switching harmonics above 250 Hz are attenuated.

Case 1: to analyze and evaluate the improvised control robustness against voltage harmonic distortion. Figure 4.1 shows simulation results of load current under distorted supply voltage condition. For distorted and uncompensated condition, 10.51 % of the fifth and 9.07 % of the seventh harmonics, respectively, 5.36 % of the eleventh and 8.37 % of the thirteenth harmonics, respectively, are subjected to the supply voltage, which results in THD of 12.06 %. Figure 4.2 shows simulation results of load voltage under distorted supply voltage condition.

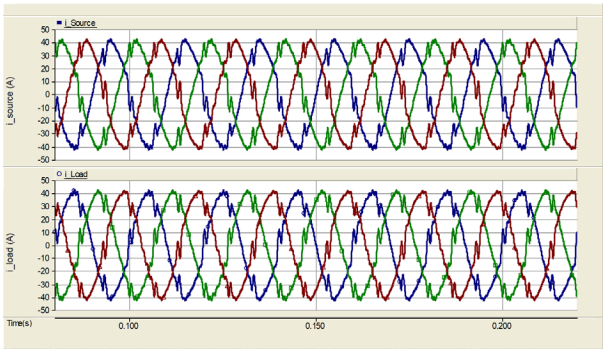


Figure 4.1. Load current under distorted supply voltage condition.

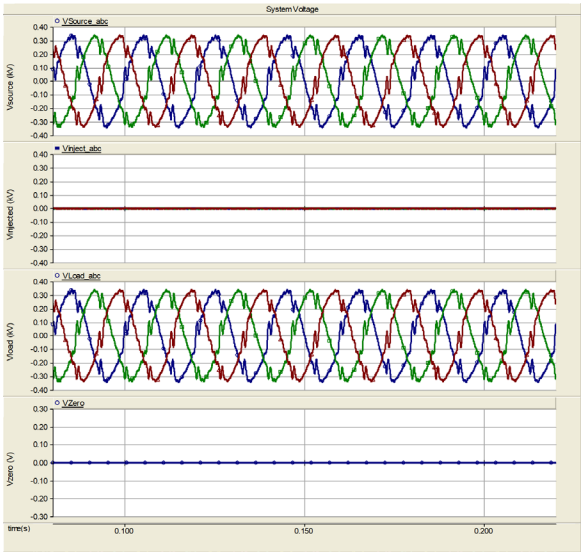


Figure 4.2. Load voltage under distorted supply voltage condition.

Figure 4.3 shows simulation results of load current after compensation. For undistorted condition, 1.19 % of the fifth and 0.71 % of the seventh harmonics, respectively, 0.82 % of the eleventh and 0.91 % of the thirteenth harmonics, respectively, are subjected to the supply voltage, and the THD of the voltage has been significantly reduced to 1.63 %. Figure 4.4 shows simulation results of load voltage after compensation.

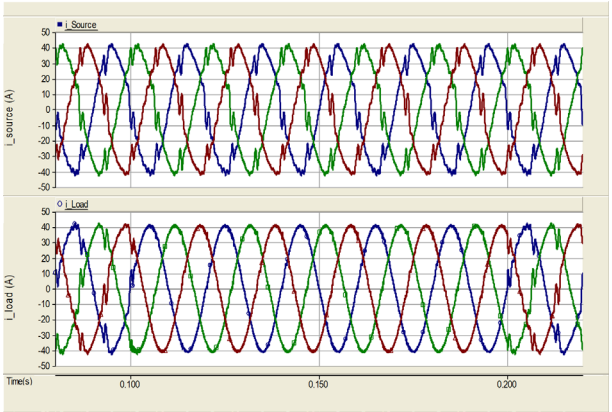


Figure 4.3. Load current after compensation.

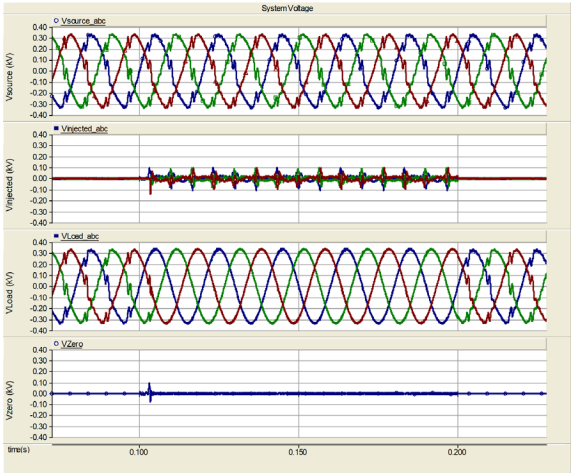


Figure 4.4. Load voltage after compensation.

Case 2: to analyze and evaluate the improvised control robustness against voltage swell. The simulation started with the supply voltage swell is generated on phases abc as shown in Figure 4.5. As observed from this figure the amplitude of supply voltage is increased about 15 % from its nominal voltage rising to 500 Volts. The same figure shows the injected and the load voltage, respectively. The DVR reacts quickly to inject the appropriate voltage component

(negative voltage magnitude) to correct the load voltage. As can be seen from the results, the load voltage is kept at the nominal value 340 Volts by the DVR.

Case 3: A single line to ground fault is applied on phase a. The healthy phases show the same magnitude. The supply voltage on phase a dropped to 200 Volts which also affected the supply phase a voltage at the sensitive load downstream. For 100 ms, the DVR starts injecting the required compensating voltage, thus restoring the voltage at the sensitive load to its rated value of 340 Volts and is sinusoidal. The results confirm the improved transient performance of the DVR. The simulated result for a single line-to-ground fault with the injected voltage and voltage at the sensitive load is shown in Figure 4.6. Table 4.0 is the summary of voltage sag and restored voltage of each phase.

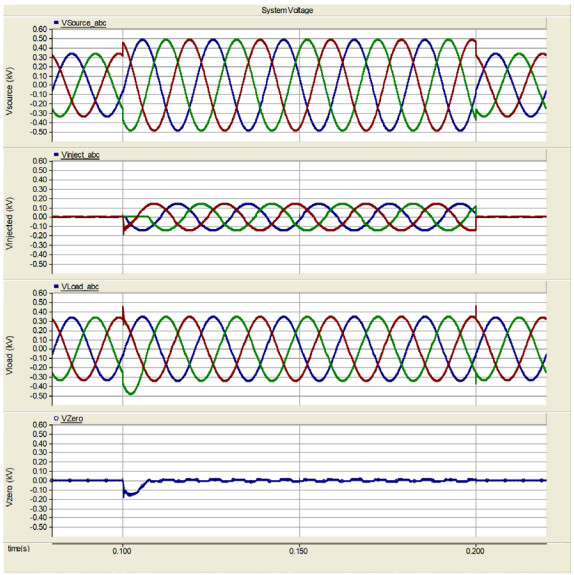


Figure 4.5. Swell mitigation by DVR

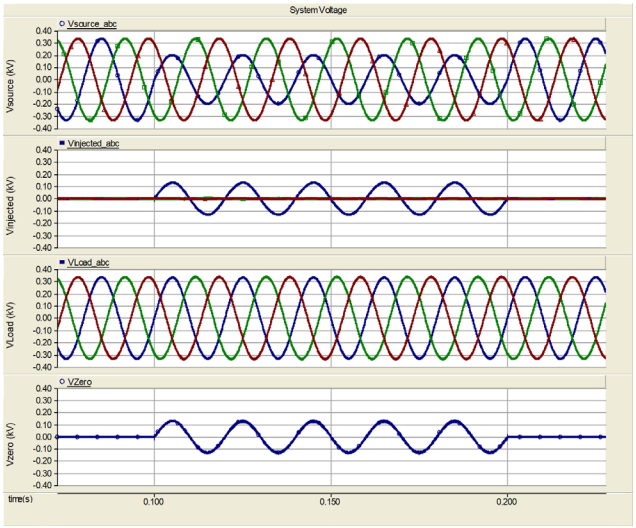


Figure 4.6. Single line to ground fault

Table 4.0. Summary of voltage sag and restored voltage

Single line to ground fault			
Phase	Voltage sag	Compensating voltage	Restored voltage
a	200 V	140 V	340 V
b	NIL	NIL	340 V
c	NIL	NIL	340 V

Case 4: A double line to ground fault is applied on phases a and b to ground. The healthy phase shows the same magnitude. The supply voltage on phases a and b dropped to 200 Volts which also affected the supply phases a and b voltage at the sensitive load downstream. For 100 ms, the DVR starts injecting the required compensating voltage, thus restoring the voltage at the sensitive load to its rated value of 340 Volts and is sinusoidal. The results confirm the improved transient performance of the DVR. The simulated result for a double line-to-ground fault with the injected voltage and voltage at the sensitive load is shown in Figure 4.7. Table 4.1 is the summary of voltage sag and restored voltage of each phase.

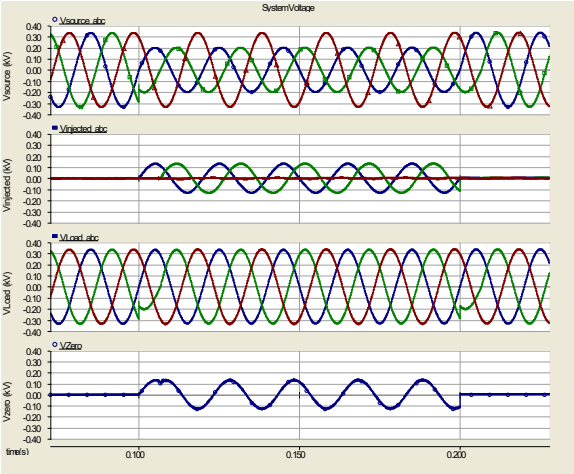


Figure 4.7. Double line to ground fault

Table 4.1. Summary of voltage sag and restored voltage

Double line to ground fault			
Phase	Voltage sag	Compensating voltage	Restored voltage
a	200 V	140 V	340 V
b	200 V	140 V	340 V
c	NIL	NIL	340 V

Table 4.2. The comparison of the related research and current investigation

Description			Current Study
Year	2012	2012	2020
Operating voltage and frequency	400 V 50 Hz	400 V 50 Hz	400 V 50 Hz
Inverter type	3-level	3-level	Cascade 7-level
RMS of the supply side voltage	240 V	240 V	240 V
RMS of the load side voltage after compensation	Not available	Not available	240 V
THD of the supply side voltage	Not available	Not available	12.06 %
THD of the load side voltage after compensation	3.9 %	4.35 %	1.63 %

5.0 Validation

A new methodology for voltage imperfection is proposed in this research. Mathematical and simulation results display the accuracy and applicability of the proposed methodology for the application. From the results it can be concluded the proposed DVR model is accurate for power quality improvements. A comparative analysis shows the THD level in the system is reduced from 12.06 % to 1.63 % compared to some classical controllers as shown in Table 4.2. The calculated output of the methodology accurately represents the voltage disturbances. The simulation results validate and justify that the proposed innovative synchronous rotating reference frame algorithm is a superior approach than the classical schemes.

6. 0 Conclusion

The foremost research is the development of an improved innovative DVR model in PSCAD platform. An improved inverter topology for the DVR that will compensate the voltage swell, voltage sag and reduce the level of voltage

harmonics. The DVR was developed with an innovative new improved control technique that is able to improve the transient and steady-state response and improve the injection capability for the mitigation of voltage swell / sag and suppression of voltage harmonics in the power distribution network. Improving the voltage injecting capability of the proposed DVR will increase the ride-through capability characteristics of the DVR both for the suppression of voltage harmonics as well as mitigation of short and deep voltage sags. The DVR has reduced the THD level at the sensitive load within the permissible limit.

7.0 References

Kannan Karthik and J.E. Quaicoe (2000), "Voltage Compensation and Harmonic Suppression using Series Active and Shunt Passive Filters", Electrical and Computer Engineering, Canadian Conference, Vol. 1. pp. 582-586, 2000.

Hideaki Fujita and Hirofumi Akagi (1991), "A Practical Approach to Harmonic Compensation in Power System-Series Connection of Passive and Active Filters", IEEE Transactions on Industry Applications, Vol. 27, Issue N0.6, November/December 1991.

Bhim Singh et.al. (2015), "Power Quality: Problems and Mitigation Techniques", John Wiley and Sons Limited, 2015.

Zhongdong Yin and Lixia Zhou (2005), "A Novel Harmonics Injecting Approach on Over Saturation Suppression of DVR Series Injection Transformer", IEEE, Power Engineering Conference, pp. 1-5, 29 Nov 2005.

Steven M. Hietpas (2000), "Automatic Voltage Regulator Using an AC Voltage-Voltage Converter", IEEE Transactions on Industry Applications, Vol. 36, No.1, pp.33-38, January/February 2000.

Sunil Kumar Gupta (2010), "Study of Major Issues and Their Impact on DVR System Performance", International Journal of Computer and Electrical Engineering, Vol. 2, No.1, pp. 105-110, February 2010.

A.Venkatakrishna (2014), "Phase Shifted and Level Shifted PWM Based Cascaded Multilevel Inverter Fed Induction Motor Drive", International Journal of Current Engineering and Technology, Vol.4, No.1, pp.350-354, February 2014.

N.H. Woodley (2000), "Field experience with Dynamic Voltage Restorer" Power Engineering Society Winter Meeting, vol. 3, pp. 1323-1328, IEEE, 2000.

Sasitharan S (2008), "Rating and Design Issues of DVR Injection Transformer", IEEE, Applied Power Electronic Conference (APEC), pp.449-455, 24-28 Feb. 2008.

Mahinda Vilathgamuwa and S.S.Choi (2002), "Performance Improvement of the Dynamic Voltage Restorer with Closed-loop Load Voltage and Current-Mode Control", IEEE Transaction on Power Electronic,Vol.17, No.5, pp. 824- 834, September 2002.

H. Tiwari and S. Kumar Gupta (2010), "DC Energy Storage Schemes for DVR Voltage Sag Mitigation System," International Journal of Computer Theory and Engineering, vol. 2, no. 3, pp. 313-318, June 2010.

Suresh Kumar (2015), "Mitigation of Lower order Harmonics in a Grid connected Three Phase PV Inverter", International Research Journal of Engineering and Technology (IRJET), Vol 02, pp. 1036-1046, Aug 2015

Corasaniti V et. al. (2009), Barbieri M, Arnera P, Valla M. "Hybrid active filter for reactive and harmonics compensation in a distribution network, IEEE Trans Ind Electron, pp.670-677, 2009.

AlirezaJavadi (2012), "A Novel Transformerless Hybrid Series Active Filter", IEEE Industrial Electronics Society, pp.5312- 317, 25-28 Oct. 2012.

8.0 Biography

K Chandrasekaran is Assistant Professor in the department of Industrial engineering at University Tunku Abdul Rahman (UTAR) Kampar, Perak. He holds a Master of Science in Electrical and Electronics Engineering from University Technology Petronas (UTP) and PhD in Engineering from University Tenaga Nasional (UNITEN). He has published in journal and conference papers. His research interests include Power Electronics, FACTS, Power Systems, and Filters. He is a Professional Engineer and Competent Engineer registered with IEM, BEM and EC, Malaysia.

V.K. Ramachandaramurthy is a Professor at University Tenaga Nasional. He is the Head of Power Quality Research Group, University Tenaga Nasional, Malaysia. He has published in journal and conference papers. He is a Professional Engineer registered with IEM, BEM, Malaysia.