DEVELOPMENT OF AN FPGA BASED LOW POWER SYSTEM FOR DISPLAYING MUSLIM PRAYER TIME

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ABSTRACT

The display elements in an embedded system usually consume the major portion of the total power required to run the whole system. When large amount of display elements are used, power dissipation issue becomes more acute. An FPGA based embedded system implementing scanning technique for low power message display is proposed in this paper. The FPGA based intelligent controller scans all the display elements continuously at a certain speed to ensure only one display unit is 'ON' and others are 'OFF' at a given time but human eye cannot detect it due to speedy scanning of the controller. Here an FPGA based embedded system for 'Muslim Calendar' containing date, time and prayer times for five salat has been developed using 30 seven segment display units. Experimental result shows that dynamic scanning makes the current consumption 88% less and power requirement 82% less than that of the static display.

Keywords: FPGA, Scanning, Message, Display and Low Power.

1. INTRODUCTION

An electronic display is a device which is used for presentation of text and images for visual reception, without producing a permanent record. The use of electronic displays for presentation of graphs, symbols, alphanumeric, and still or video pictures has doubled every several years, in parallel with the rapid expansion of microelectronics [1-3]. Electronic displays have largely replaced traditional mechanical devices, counters, galvanometers, and to a degree, hardcopy (paper) means for presenting information. This change is due to the increased use of computers, microprocessors, very large-scale integration (VLSI) electronics, and digital mass memories. Electronic display-we see it everywhere, in computers, watches, DVD players and many other electronic devices to display numeric and alphabetic characters [4-8]. It is also used for showing messages in digital calendars, billboards, shopping malls, airports, stadiums and many other places. It is a commonly used and efficient way of displaying information. Although electronic display is widely used, power consumption is still an important issue [9-12].

Portable embedded system is a vision of this day. It is usually a battery operated electronic products. Low power dissipation is a desirable and/or even essential in these equipments to have reasonable battery life and weight of the system. In an electronic system having display elements, the major part of the total power is consumed by the display elements. If a large amount of display units are used in a system then the power requirement to run the system will also increase proportionately. In that case extra cooling arrangements may be required to keep the system workable. Researchers have proposed plasma screen or organic light-emitting devices (OLED) to reduce power consumption for display element [13-14]. A microcontroller (μC) based system using scanning technique is proposed for low power message display by previous researcher [15]. In that paper a Muslim Calender for displaying date, time and five prayer time for salat was developed using seven segment display. A microcontroller based system is usually burdened with the problem of limited number of pins, limited physical security and slow processing speed. Seven segment display with integrated controller and other circuitry are proposed to reduce the burden from main controller [16-17]. But in this case cost will be increased and power will be consumed by display control circuitry. Now the Field Programmable Gate Array (FPGA) technology outperforms microcontroller

technology and offers improved performance, reduced power consumption, reduced system size, more physical security and shorter time to market. Besides this FPGA has parallel processing feature to enhance the speed performance. So it is widely used in many applications. In this research paper, FPGA has been used replacing the microcontroller technology to enhance the performance of the system as shown in the literature [15].

2. SCANNING TECHNIQUE

This paper concentrates on the power dissipation issues for display devices. A scanning technique has been introduced in the proposed system to minimize the power consumption for display elements. The objective is to connect all the display elements in parallel with each other and turning only one unit 'ON' at a time for a very short period and move to the next unit. If each unit can be illuminated periodically in a very short span of time the human eye will see the entire message as if all the units are turned 'ON' whereas only one unit is ''ON at any given time.

Here seven segment displays are used as display units and as a test case a Muslim Calendar (displays Date, Time and Prayer times of Five Salah) is developed using 30 units of seven segment display. ULN is used to select the corresponding display unit. ULN is a very fast device to turn "ON" and turn "OFF" of display units. As the algorithm for illuminating display units follow the scanning technique where only one unit of seven segment display is turned ''ON at any given time. So, theoretically the total power consumption for illuminating display units is reduced by 30 times. Hence 30 units of seven segment displays can be illuminated by only the power required by one unit.

3. ARCHITECTURE OF THE SYSTEM

The basic units of the proposed system can be divided into 6 parts: FPGA, Display elements, Display Decoder (CD4511BE), ULN (2803), Power Unit and Switches.

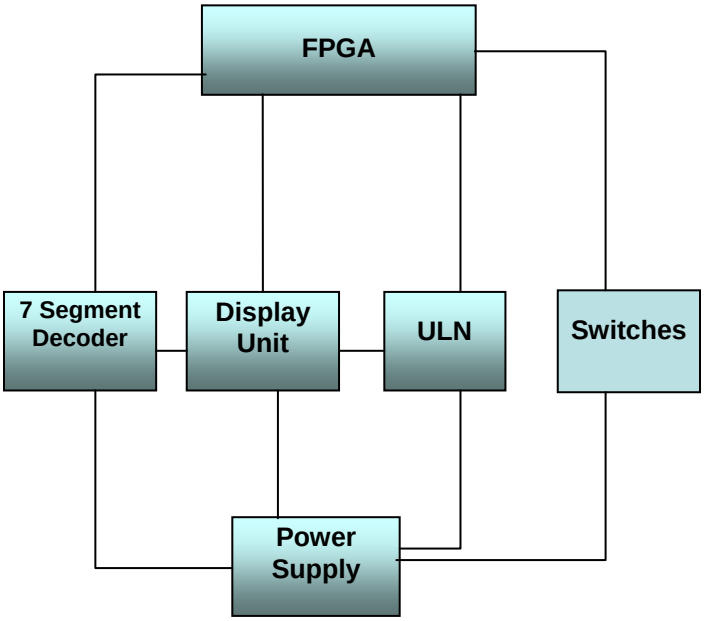

Figure 1: Block diagram of the system

The outputs of the ULN are connected to the common cathodes of 30 seven segment displays. The FPGA initializes all the output pins of the ULN (sends logic 1 thirty times in the input of the ULN), making all the seven segment displays to be turned 'OFF'. At this point the FPGA sends logic 0 once and logic1 29 times so that each display receives the signal 0 sequentially while other displays receive signal 1. In this process, only one display unit is turned 'ON' at a time and shifted sequentially.

The output pins of the Seven Segment Decoder are connected in parallel to all seven segment displays. The FPGA sends appropriate input data for the decoder when corresponding seven segment display has logic 0 at its common cathode. The prayer times change with the change of day and month field of the date. Three switches are used to set time and date. One switch is used to select which field of the time and date is to be changed. Other two switches are used to count up and count down the selected field. All these operation is controlled by the FPGA.

The main part of the system is the FLEX EPF10K70RC240-4 FPGA. All other components are connected to it and controlled by it. The four input pins of the seven segment decoder (CD4511BE) are connected to the first four pins of the FPGA. The input pins of the ULN are connected to the pins of FPGA. All output pins of ULN are connected to the common cathode pin of the 7 segment display sequentially. A 25.175MHz crystal oscillator is connected to the pin 91 of FLEX 10K FPGA.

4. OPERATION OF THE SYSTEM:

In the proposed system a controller scans all the display units continuously to ensure that only one unit is on at any given time. In this way power consumption will be much lower than that of existing static display system. Here a 'Muslim Calendar' containing date, time and prayer times for five salat has been developed as a test case. Seven segment displays are used as display units.

Here the FPGA controls the input of the ULN and Decoder. The FPGA initializes all the output pins of the ULN at level 1 (sends logic 1 thirty times in the input of the ULN), making all the seven segment displays to be turned 'OFF'. At this point the FPGA sends logic 0 once and logic1 29 times so that each display receives the signal 0 sequentially while other displays receive signal 1. In this process, only one display is turned at a time and shifted sequentially.

5. SIMULATION:

The system is simulated using the Quartus II 7.0 simulator. The overall simulation is done using to the EPF10K70RC240-4 FPGA. Figure 2 shows the simulation of decoder data with counter. The counter is reset when its counter value becomes 30.

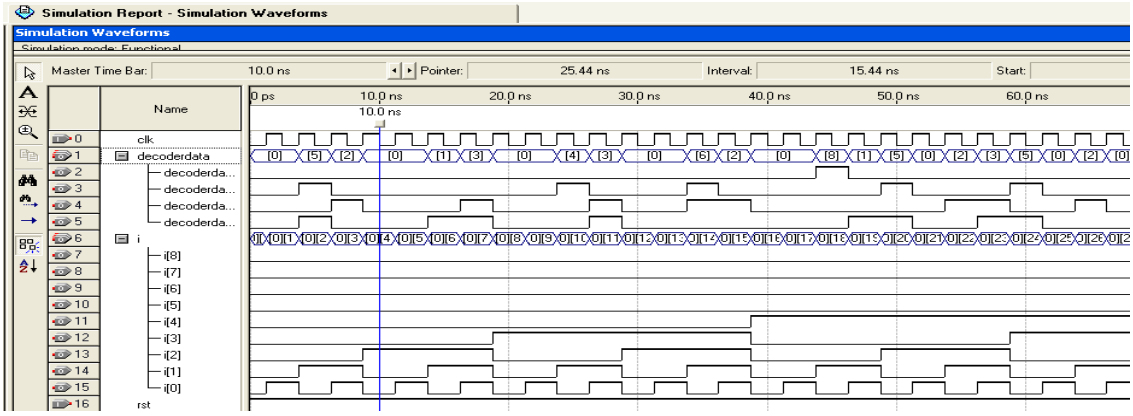

Figure: 2 Counter and decoder data simulation

Figure 3 shows the overall simulation of the proposed system. The overall simulation is done using to the EPF10K70RC240-4 FPGA.

It can be seen from the simulation that when one ULN passes signal LOW to the common cathode of a particular seven segment display at that time all other ULN passes the HIGH signal to the common cathode of the others seven segment display. When a seven segment display gets LOW signal in Common Cathode then it show the corresponding data passes by seven segment decoder. Seven segment decoder gets input from FPGA controller and passes to seven segment display. Seven segment display is controlled by ULN.

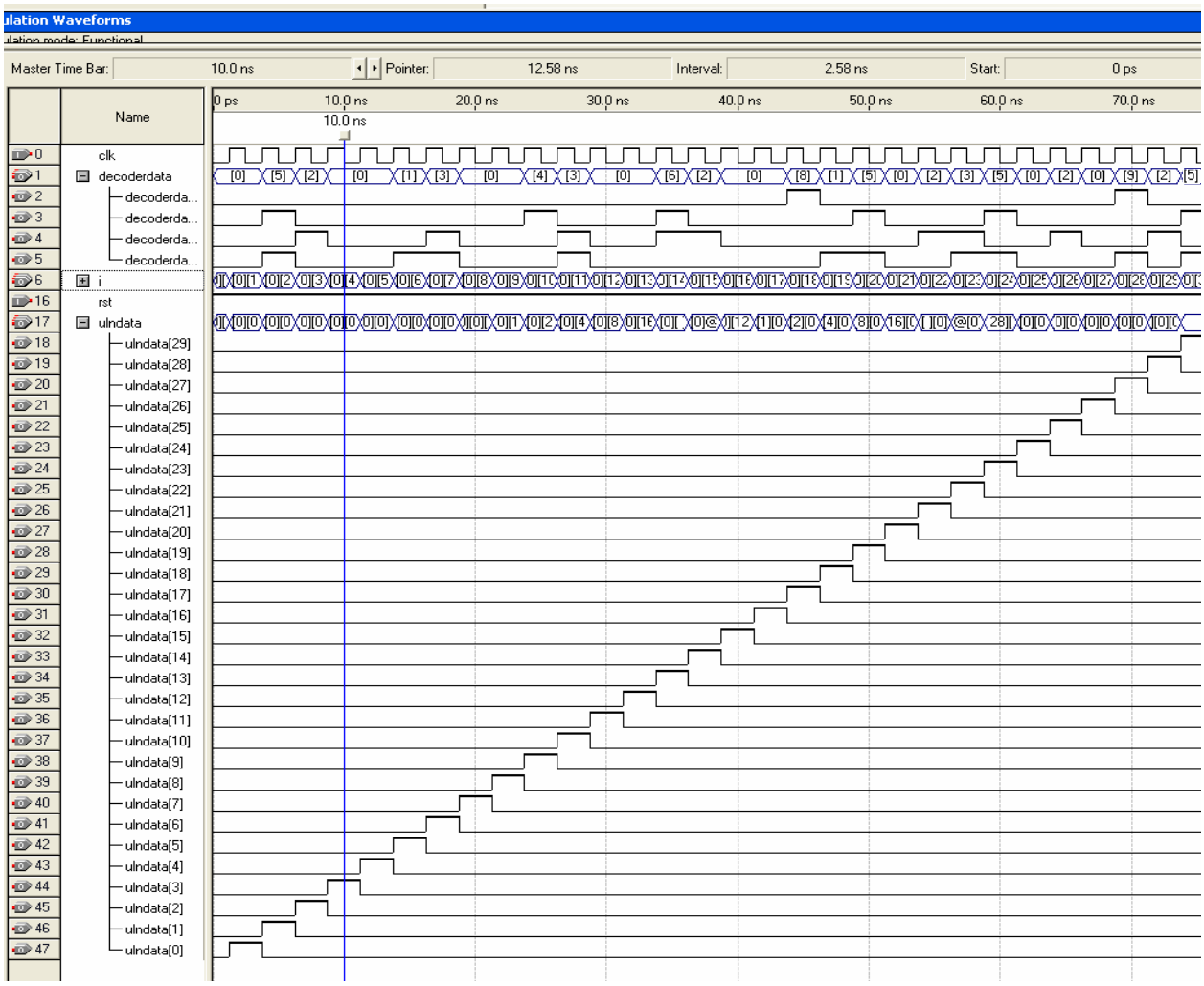

Figure 3: Overall Simulation Result

The simulation result shows that when ULN no. 01 passes 0 signal to Display unit no. 01 then only Display unit no. 01 will be 'ON' in that time all other display unit will be 'OFF'. For a particular signal of ULN a particular data is shown in a corresponding seven segment display unit.

6. ARTVIEW OF THE PROPOSED SYSTEM:

After putting all the components on the circuit board and programming the FPGA the whole system looks like Figure 4.

Here the first block of six (top) seven segment displays shows time. First two units of this block represent hour while second two represent minute. The third two represents seconds. The second block of four (top Left corner) seven segment displays represents date where the first and second two units of the block represent month and day respectively. The remaining five blocks of four seven segment displays represent the prayer times of five salat; Fazr, Zurh, Asr, Maghrib and Esha as labeled in Figure 4. Here each first two units of each block represent hour and the remaining two units of each block represent minute.

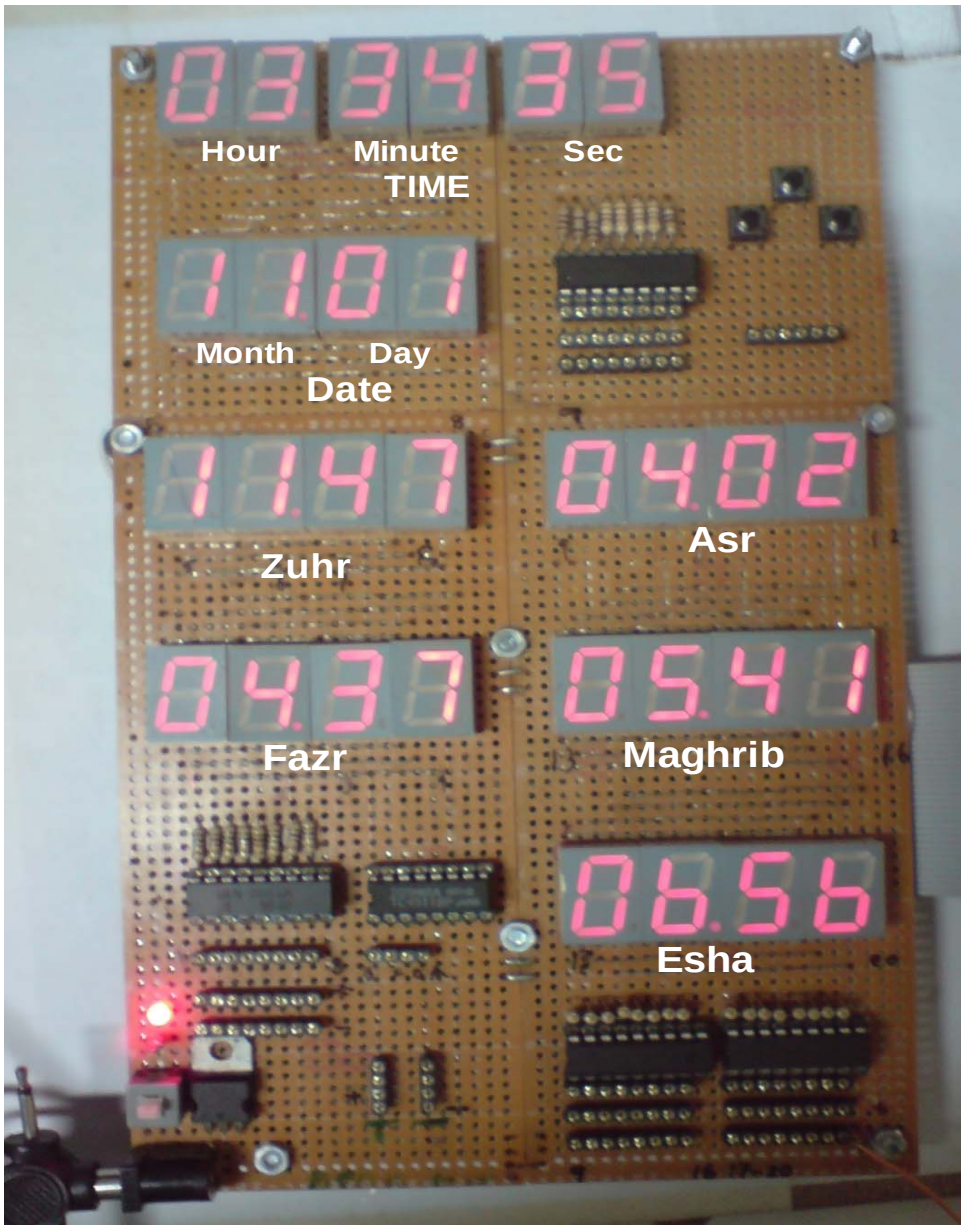

Figure 4 Artview of the Proposed System

7. POWER AND CURRENT CONSUMPTION

Scanning technique is a power aware solution for message display. Here we have used 30 seven segment display units. But as scanning technique is applied, at any given time only one seven segment display is 'ON'. So, theoritically the system should consume 1/30 times less power than it would take to make all the seven segment displays 'ON' at a time.

Power Analysis of the FPGA based system has been carried out using the power analyzer tool of the Quartus II. It shows that the required power for design is 33.25 mW. In the laboratory an experiment has been conducted to measure the current and power for the developed system. To find the current and power consumption of the system in the worst case without scanning technique all the segments have been enlighted and then power and current are

measured. In the similar way the current and power for the system with scanning technique are also measured for the worst case situation. Table 1 shows the experimental results.

Table 1 Current and Power Consumption of the system

	With Scanning Technique	Without Scanning Technique
Current Consumption	0.008 A	0.070 A
Power Consumption	0.070 W	0.383 W

It is observed from Table 1 that it is possible to reduce 88% less current and 82% less power consumption using FPGA based scanning technique.

8.COMPARISON OF THE PRESENT WORK WITH THE OTHER RESEARCH

The present work consumes less current and less power than the work of Khan, M. R.[15]. A comparison study between present research and previous research is presented in Table 2.

Table 2 Comparison of Current and Power Consumptin with the work of Khan, M. R.[15]

	Current Consumption	Power Consumption
Khan, M. R.[15]	0.018 A	0.090 watt
Present Work	0.008 A	0.070 watt

It can be observed from Table 2 that the present work requires 55% less current consumption and 22% less power than the work of Khan, M. R.[15].

Since the present work is FPGA based design, it removes the pin limitation problem of microcontroller based design. It is also more secured than microcontroller based design. Moreover in the FPGA based system all the discrete digital components can be put in the single chip and so PCB area for the system will be less than the microcontroller based system which turn will reduce the system size, weight and cost.

9. CONCLUSION AND FUTURE WORKS

Low power embedded system offers a lot of advantages such as portability, longer battery life and compact size. To overcome the limitations of a previously developed microcontroller based embedded system for Muslim Calender was the core objective of this research. The limitations were limited number of pins, lower processing speed, lower physical security and power consumption. To improve the overall performance of the system, scanning technique has been implemented in the FPGA platform. FPGA technology eliminates limitations of pins, offers higher processing speed and physical security over microcontroller based system. EDA simulation result shows the proper functionality of the system. The laboratory test result of the system proves the significant improvement in power reduction over the existing approach. The system will be reduced in size and cost effective. It is also capable of driving larger number of display units.

The author recommends the following suggestion to improve the proposed work.

1. The work presented in this paper, Altera's Flex 10K FPGA has been used. Currently the FPGA vendors have cool runner version of FPGA for low power applications. It can be used to reduce the total power of the proposed system.
2. The Muslim Calendar in this paper only displays the prayer time at Dhaka city. It can be improved to make it universal so that it can be able to display the prayer time of any important city in this world.

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