Simulation and Design of Parameterized Convolutional Encoder and Viterbi Decoder for Wireless Communication

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Abstract

This paper focuses on Simulation and Design of Parameterized Convolutional Encoder and Viterbi Decoder Using Coding rate, Trellis length as parameter. In wireless communication high coding rate transmission is reliable but takes more time to decode comparing low coding rate. Long Trellis Length causes the Viterbi algorithm to take more time but reliable compare with short Trellis length. These combined effects are taken as consideration for design and Implementation. Using 1/2, 1/3 coding rate and 4, 15 Trellis length four different convolutional encoder and Viterbi Decoder is implemented using FPGA. Simulation is done using Quartus II 7.0.

Key Words: Convolutional Encoder, Viterbi Decoder, Humming Distance, Trillis Length, Code Rate.

1. Introduction

In wireless communication AWGN (Additive White Gaussian Noise) properties of most of the communication media introduce noise in real data during transmission. The approach to error correction coding taken by modern digital communications system starts with the ground breaking work of Shannon, Hamming and Golay [1-3]. Channel Coding is a technique to introduce redundant code in real code to remove interference and error during transmission. Coded data in sender side thus increased by volume and error effect becomes less compare with uncoded data. Receiver end receives this data and decodes the data using some techniques. Viterbi decoding is one of the popular techniques to decode data effectively. Viterbi algorithm (VA) is an optimum decoding algorithm for the convolutional code. Convolutional encoding and Viterbi Decoding are widely used for reliable data transmission. There are different approaches of implementation for Convolutional Encoder and Viterbi Decoder in the literatures [4-7]. Literature [4] presents the implementation of Convolutional Encoder and Viterbi Decoder in the DSP Platform. It is a flexible platform but slow in speed. To overcome the performance issue of Convolutional Encoder and Viterbi Decoder, FPGA based implementation has been proposed [5-7]. These Implementations have Fixed Constraint Length and Code Rate or with Partial Configuration Facility. Complexity of Viterbi decoding algorithm increases in terms of convolutionally encoded trellis length. Increasing the trellis length causes the algorithm to take more time to decode. This will cause transmission speed lower but make the transmission more reliable. Lowering the trellis length will increase the transmission speed [5] A highly complex Viterbi Decoder someway loses its advantages, when it is adopted to decode sequences transmitted on a low-noise channel. In this case, low minimum distance codes are more suitable for achieving a good performance, and a higher bit rate can be transmitted by lowering the coding rate [6]. Implementation of Convolutional Encoder and Viterbi Decoder is done separately considering the different coding rate and trellis length. Using μC Platform implementation of Convolutional Encoder and Viterbi Decoder is Slow.

2. Effect of Coding Rate

High Coding rate expands the original code with large amount of redundant data where the low coding rate data has small amount of redundant data. This has significant effect in coding, decoding and transmission media. 1/2 code rate data will need less amount of time and memory compare with 1/3 code rate. Error induced during transmission will be relatively small in high coding rate. As error gap expanded compare with low coding rate decoder will perform better on tracing the error.

3. Effect of Trellis Length

When error arises in received signal, decoding sequence expanded using binary tree structure. Each node has two paths .When last leaf level is fulfilled, maximum humming distance coded sequence in a node is kept another is discarded. Thus increasing the trellis length does not follow the complete binary tree structure after reaching the last leaf level.

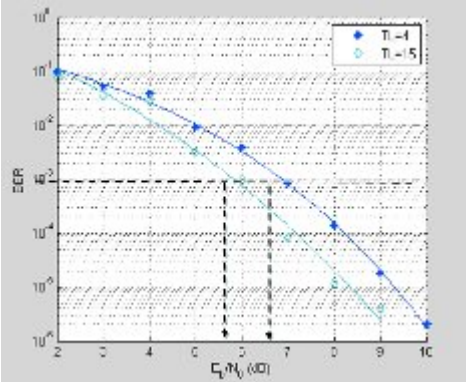

Figure 1: System performance for Trellis Lengths of 4 and 15 [5]

Maximum weighted path is taken as desired sequence. Algorithm has to expand until the trellis length is completed. This will cause the decoder to take more time when long trellis length exist. Using long trellis length error probability will decrease as decision is taken according to the cumulative sum of path weight and after long time initialization of decoding algorithm using the root node of the tree is done. Thus low error rate with high decoding time occurs. Using small trellis length causes the decoder to complete the path with sort time but initialization of decoding algorithm is done too frequently. This causes high error rate with low decoding time.

4. Convolutional Encoder

A convolutional code introduces redundant bits into the data stream through the use of linear shift registers. Convolutional codes are commonly specified by three parameters; (n,k,m). The information bits are input into shift registers and the output encoded bits are obtained by modulo-2 addition of the input information bits and the contents of the shift registers. The connections to the modulo-2 adders were developed heuristically with no algebraic or combinatorial foundation. Convolutional codes are commonly specified by three parameters (n,k,m)

n = number of output bits
k = number of input bits
m = number of memory registers

The quantity k/n called the code rate is a measure of the efficiency of the code.

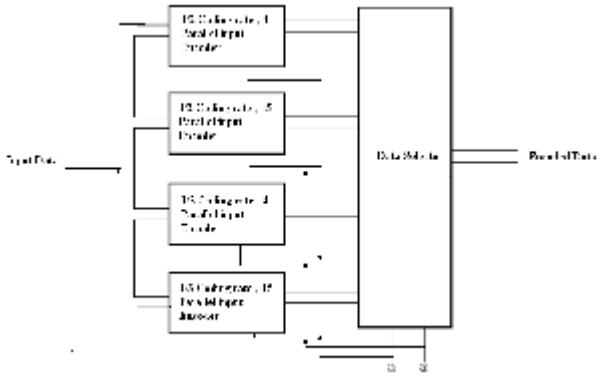

Figure 2: Convolutional Encoder Group

Using Verilog HDL four convolutional encoder with following Parameters are created.

Table 1: Parameter used to design encoder and Decoder

Constraint Length	Coding Rate	Trellis Length
4	1/2	4
4	1/2	15
4	1/3	4
4	1/3	15

Selection variable S1 and S0 is used to select different module of convolutional Encoder and corresponding output of this module is taken to transmit. Internal Calculation of each module will be activated after receiving the predefined selection bit combination. The module without valid bit combination will always output '0' bit.

5. Viterbi Decoder

The Viterbi decoder examines an entire received sequence of a given length. The decoder computes a metric for each path and makes a decision based on this metric. All paths are followed until two paths converge on one node. Then the path with the higher metric is kept and the one with lower metric is discarded. The selected paths are called the survivors. For an N bit sequence, total numbers of possible received sequences are 2^N . Of these only 2^KL are valid. The Viterbi algorithm applies the maximum-likelihood principles to limit the comparison to 2 to the power of kL surviving paths instead of checking all paths. The most common metric used is the Hamming distance metric. This is just the dot product between the received codeword and the allowable codeword.

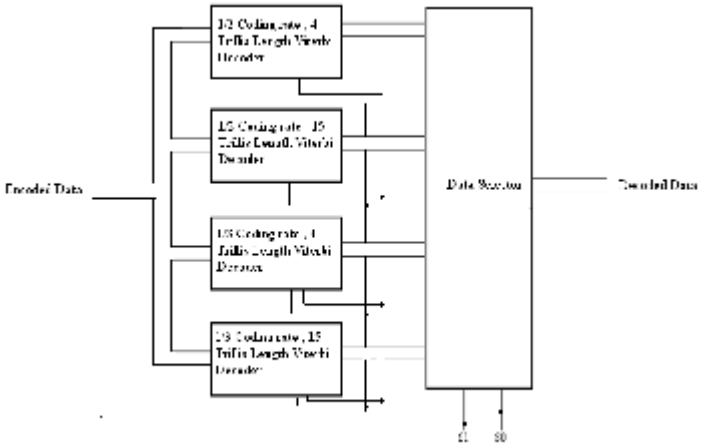

Figure 3: Viterbi Decoder Group

Four parallel module of Viterbi Decoder is designed in proposed system. Verilog HDL Provide Task and Function facility to modularize the large Design. Each decoder module is sub divided into different tasks and function. Next State Generator, Humming Distance Calculation, Branch Matrices calculation all this are implemented using task and function. S1 and S0 Selection variable are used to select different Viterbi Decoders. This Decoder selection variable has one to one relation with Encoder selection variable. Cyclone II FPGA provides 18 DPDT switches, 18 Red User LEDs. 15 DPDT switches and 15 Red User LEDs are used for Input and output purposes.

Block diagram shows different functions designed to modularized the total system. Using Random Error Generator errors in different bit position are introduced in decoder output data. Next State Generator function used this erroneous data in sequential manner combining 2 bits for 1/2 code rate and 3 bits for 1/3 code rate . This combined bits are compared with '0' output comparator and '1' output comparator and path matrix with path weights are generated. After completing the pattern matching Maximum weighted path finding function is used to find the best survival path.

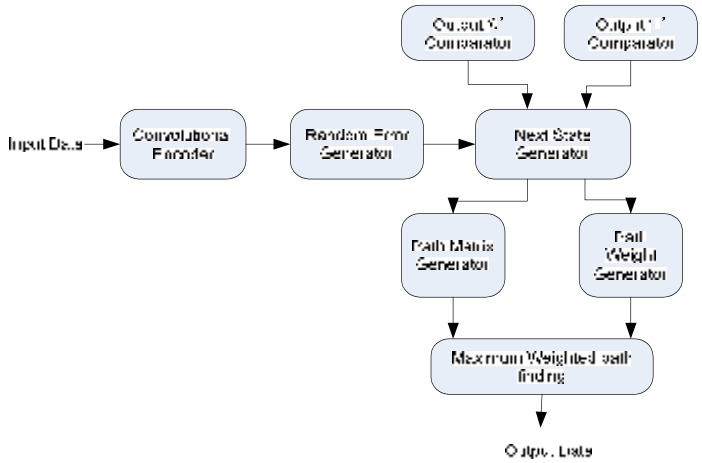

Figure 4: Block Diagram of Encoder and Decoder

6. Simulation Result

Quartus II 7.0 web edition is used for simulation of entire design. Simulation is done using timing diagram. Here idata is input data in binary format. odatatwo , odatathree is for rate 1/2 and 1/3 encoding output. rst is used to select different coding rate and trellis length. rst is three bit and MSB of rst is always high when the system is in operation

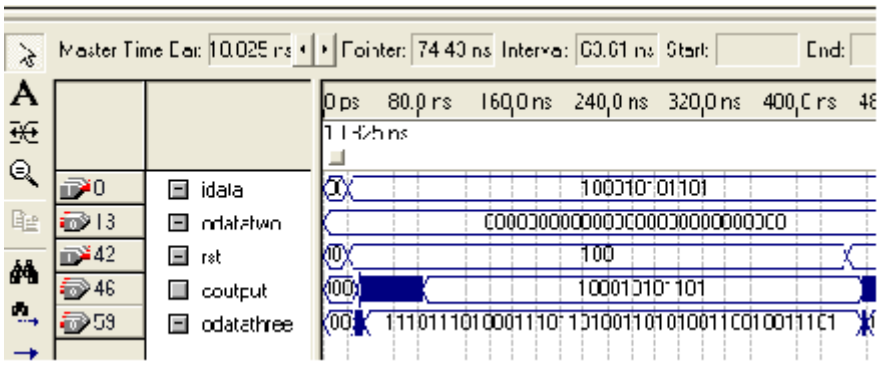

Figure 5: coding rate 1/3 , trellis length 15

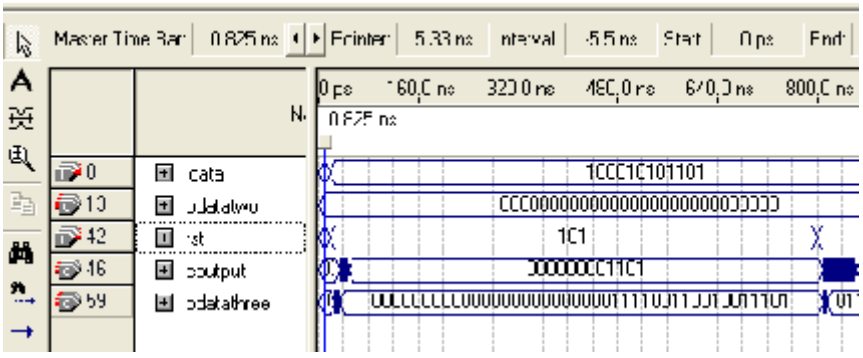

Figure 6: coding rate 1/3 , trellis length 4

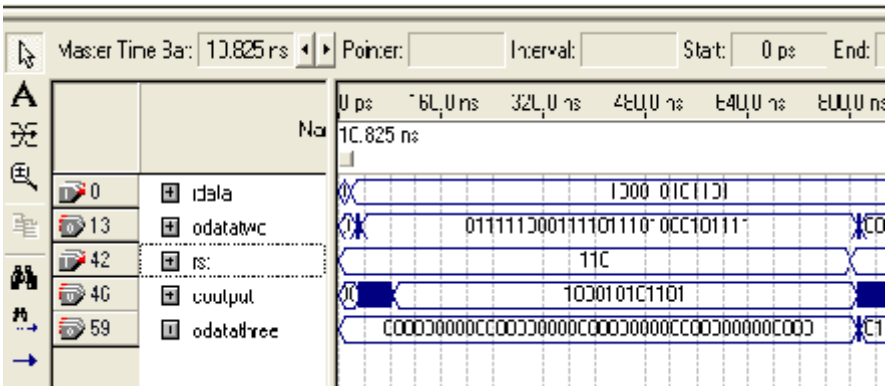

Figure 7: coding rate 1/2 , trellis length 15

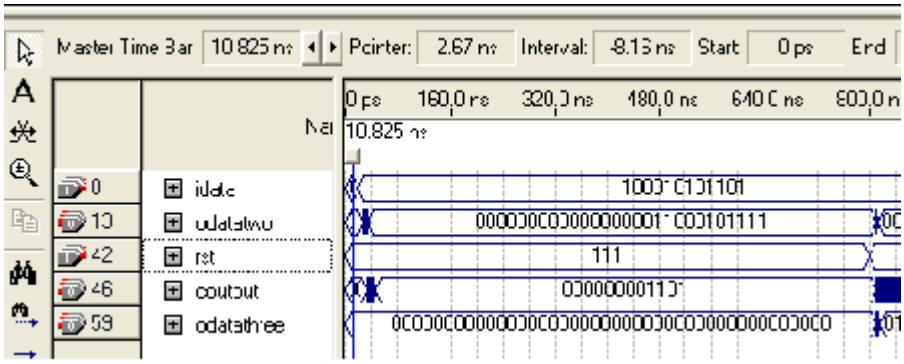

Figure 8: coding rate 1/2 , trellis length 4

7. Comparison

Previous different approaches to implement the convolutional encoder have limited configuration facility. According to the demand of environment and error recoverability significant configuration facility is introduced in proposed system. The proposed system is fully code base using verilog modularized facility of task and function. Thus the system can be easily expandable compare with other once making the copy of code and slight change in it. A tabular comparison of different system of Implement is given below

Table 2: Comparison of different Implementations.

Research work	Variable Trillis Length	Variable Code Rate	Speed
DSP	No	No	Slow
Micro Controller	No	Yes	Slow
Xilinx XCV300PQ240-4 FPGA	No	Yes	Fast
Xilinx Virtex-II Pro.XC2vp30 FPGA	Yes	No	Fast
Cyclone II EP2C35F672C6	Yes	Yes	Fast

8. Area Usage

Cyclone II FPGA has total 33216 logic Cell . Among this only 15.2871 % is used for implementing this Encoder and Decoder. Area usage for each module is given bellow

Table 2: Device utilization of Cyclone II FPGA

Module	Code Rate	Trellis Length	Logic Cell	Percent of total Logic Cell
Encoder	1/3	15	6	0.0180 %
Encoder	1/3	4	3	0.0090 %
Encoder	1/2	15	13	0.0391 %
Encoder	1/2	4	3	0.0090 %
Decoder	1/3	15	2212	6.6594 %
Decoder	1/3	4	281	0.8459 %
Decoder	1/2	15	2327	7.0056 %
Decoder	1/2	4	116	0.3492 %

9. Conclusion

This Paper Highlights the Simulation and Design of Different Convolutional Encoder and Viterbi Decoder using Code rate and Trillis Length as parameter. Changing this parameter has significant effect during transmission. Using Verilog HDL all decoders and encoders are designed in different module. Only 15.2871 % of total Chip area is occupied by this design, which imply that the design can be expanded with more variation.

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